VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph at page 6, line 22 has been amended as follows:

FIGURE 1C shows a fragmentary cross-sectional view of an alternate embodiment in which the leads 50 [50'] are located on the same side as the terminals 40; thus, not requiring the conductive vias 70 (shown in **FIGURE 1B**). A solder mask/coverlay is also used in the embodiment shown in **FIGURE 1C** because the leads 50 and the terminals 40 are on the same side of the substrate 30. The solder mask/coverlay provides a dielectric coating ensuring that the solder connecting the terminals to contacts on the printed circuit board does not wick down the leads or short to other soldered terminals.

The paragraph at page 8, line 3 has been amended as follows:

A die attach material 80' [80] is provided over the die 10, and a solder ball array 40 is provided over the die attach material that serves to make the connection to the next-level package. The solder balls 40 are preferably relatively flexible and can thus compensate for any lack of flatness in the printed circuit board or package. Additionally, the solder balls are assembled in an array, and thus provide a relatively high throughput. In one preferred embodiment, the solder balls are made of a SnPb eutectic material such as Sn63Pb37 and have a diameter of about 0.3 to 0.5 mm. The bump pitch on the tape can be as small as about 0.25 to 1 mm, and is more preferably about 0.5 mm.

The paragraph at page 8, line 12 has been amended as follows:

Tape 50' [50] extends over the die attach material forming a connection with the solder ball array 40. TAB leads 55' [55] extend from the tape 50' [50] to form a connection with the die 10 at die pads 20. The tape 50' [50] preferably comprises a conductive material such as copper for connecting a die pad 20 to a solder ball 40, and a polyimide material to connect the solder balls. The tape 50' [50] preferably has a thickness of about 50 μm.

The paragraph at page 8, line 17 has been amended as follows:

FIGURE 3 illustrates in cross-section a close-up view of the first level package 8 of **FIGURE 2**. Leads 55' [55] are preferably ultrasonically bonded to the die 10 at die pads 20 (not shown). The point where the leads 55' [55] contact the die 10 is the heel 86.

The paragraph at page 8, line 20 has been amended as follows:

The die attachment layer 80' [80] can be made from an epoxy modified with elastomeric material used to prevent breakage of the leads 55' [55] from the die 10 at the heel 86 (the heel break). The thickness of the layer is preferably about 3 to 9 mils, more preferably about 5 to 7 mils. In one embodiment, the die attachment layer has a modulus of elasticity of about 126 ksi at room temperature. This die attachment layer preferably has a glass transition temperature T_g of about 42°C, a coefficient of thermal expansion (CTE) of about 106 ppm/°C or less below T_g, and a CTE of about 234 ppm/°C above T_g. Such a material is available from Ablestik Lab of Rancho Dominguez, California, No. RP 559-2A.

The paragraph at page 9, line 4 has been amended as follows:

For instance, the die attach layer 80' [80] is designed to have a low CTE in order to minimize the amount of expansion and contraction of the layer, especially relative to the die 10 and the tape 50' [50], thereby preserving the connection between the die 10 and the leads 55' [55] at the heel 86. This is important because the package 8 may undergo temperature cycling, for example, between -55 and 125°C, for up to 1000 cycles or more.

The paragraph at page 9, line 10 has been amended as follows:

In one embodiment, the die or chip 10 has a CTE of about 3 ppm/°C and the tape 50' [50] has a CTE of about 20 ppm/°C. The CTE of the tape 50' [50] is the "effective CTE" of the combined layers forming the tape. Thus, as compared to the prior art, it has been discovered that a die attach layer 80' [80] with a CTE closer to that of the die and the tape is desirable, preferably less than 200 ppm/°C, more preferably less than 150 ppm/°C. In the embodiment described above, it has been found that a CTE of less than about 100 ppm/°C is sufficient to alleviate the heel break problem. The reduced movement of the die attach layer 80' [80] because of the low coefficient of thermal expansion reduces the risk of breakage of the leads 55' [55] at the heel 86.

The paragraph at page 9, line 19 has been amended as follows:

While the die attach layer preferably has a low coefficient of thermal expansion, the present inventors have found that the layer should still be sufficiently compliant to absorb stresses between the die 10 and the solder balls 40. However, as compared to the prior art, in one embodiment, the modulus of elasticity of the die attach layer 80' [80] is selected to be

higher than that of previous die attach layers. Thus, wherein some prior art die attach layers have a modulus of less than 10 ksi, one embodiment of the present invention provides a die attach layer with a modulus of greater than about 10 ksi, more preferably greater than about 50 ksi, even more preferably greater than about 100 ksi, and in one embodiment, up to about 126 ksi. The higher modulus provides improved resistance to movement in the die attach layer, thereby decreasing the amount of stress concentrated at the heel 86. At the same time, the modulus of the layer 80' [80] is still sufficiently compliant to reduce the amount of stress applied to the solder balls 40.

IN THE CLAIMS

Claims 9, 12, 13, 14, 16, 17, 21 and 25 have been amended as follows:

9. (Amended) The integrated circuit package of Claim 8, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

12. (Amended) The integrated circuit package of Claim 8, wherein the [package includes] array is a ball grid array.

13. (Amended) The integrated circuit package of Claim 8, wherein the [package includes] array is a tape ball grid array.

14. (Amended) The integrated circuit package of Claim 8, wherein the [package includes] array is a micro ball grid array.

16. (Amended) The integrated circuit package of Claim 15, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

17. (Amended) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip

wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip.

21. (Amended) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip;

wherein the adhesive layer has a modulus of elasticity of greater than about 10 ksi and less than about 126 ksi.

25. (Amended) An integrated circuit package, comprising:

a flexible substrate;

a chip;

a plurality of conductive terminals on the substrate;

a plurality of conductive leads electrically connecting the conductive terminals to the chip; and

a compliant material between the chip and the substrate, the compliant material having a modulus of elasticity of less than about 126 ksi at room temperature and a coefficient of thermal expansion of less than about 200 ppm/°C.[The integrated circuit package of Claim 25, wherein the flexible substrate is a polyimide.]